IN THE SPECIFICATION

Please replace the titled as shown below.

~~MONOTONOUS~~ MONOTONIC COUNTER USING MEMORY CELLS

Please replace the paragraph beginning on page 1, line 6 as shown below.

The present invention relates to the field of counters and, more specifically, to ~~monotonous~~ monotonic counters with an irreversible count variation in a single direction.

Please replace the paragraph beginning on page 1, line 10 as shown below.

Currently, to form ~~monotonous~~ monotonic up-counters, fuse elements have to be used, which have the major disadvantage of causing a destructive programming often incompatible with a programming during operation of the integrated circuit containing the fuse element. Another example relates to EPROM or EEPROM memories, the manufacturing of which requires steps not directly compatible with a CMOS technology.

Please replace the paragraph beginning on page 1, line 30 as shown below.

The other one-time programming memory cell techniques which would be likely to be used in ~~monotonous~~ monotonic counting operations are in practice inexploitable. For example, cells of fuse or anti-fuse type require programmings by destructive currents which are often incompatible with the product being manufactured.

Please replace the paragraph beginning on page 2, line 3 as shown below.

The present invention aims at providing a ~~monotonous~~ monotonic counter which overcomes the disadvantages of conventional counters.

Please replace the paragraphs beginning on page 2, line 8 as shown below.

The present invention also aims at providing a solution to form a ~~monotonous~~ monotonic counter, the counting of which is compatible with the operation of an integrated circuit.

The present invention also aims at providing the forming of a ~~monotonous~~ monotonic counter by using conventional MOS-type manufacturing technologies.

To achieve these and other objects, the present invention provides a ~~monotonous~~ monotonic counter formed as an integrated circuit, each counting bit being provided by a memory cell containing at least one ~~memorization~~ storage element formed of a polysilicon resistor, programmable by irreversible decrease in its value.

Please replace the paragraphs beginning on page 3, line 26 as shown below.

~~Same~~ The same elements have been designated with the same reference numerals in the different drawings. For clarity, only those elements that are necessary to the understanding of the present invention have been shown in the drawings and will be described hereafter. In particular, what exploitation is made of the counting results has not necessarily been detailed, the present invention being implementable whatever the destination of the counting result, provided that an irreversible ~~monotonous~~ monotonic counter is desired.

A feature of the present invention is to form a ~~monotonous~~ monotonic counter based on as many counting cells as the counter comprises bits. Further, according to the present invention, the ~~memorization~~ storage element of each counting cell is formed of a polysilicon resistor programmable by irreversible decrease in its value. This feature of the present invention will appear from the following discussion of Figs. 1 and 2, which illustrates the programming possibilities of a polysilicon resistor exploited by the present invention.

Please replace the paragraph beginning on page 13, line 24 as shown below.

An advantage of the present invention is that it enables forming a perfectly reliable ~~monotonous~~ monotonic counter, the programming of which does not go along with a destruction of the counting cells.

Please replace the paragraph beginning on page 13, line 31 as shown below.

The example of Fig. 6 shows the case of an increasing ~~monotonous~~ monotonic counter. It should however be noted that, according to the decoding circuit used, a decreasing count can be obtained.

Please replace the paragraph beginning on page 14, line 16 as shown below.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, the present invention applies whatever exploitation is made of the obtained count. Further, the dimensions to be given to the different resistors, transistors, and supply and read voltages are within the abilities of those skilled in the art based on the functional indications given hereabove and on the desired application. Further, the number of bits provided in the counter is not limited. Finally, other counting cell structures than those illustrated in Figs. 3 to 5 may be envisaged, provided to respect the use of at least one resistive ~~memorization~~ storage polysilicon element, programmable by irreversible decrease in its value. One may in particular be inspired from a conventional memory cell structure, adapting it to the use of such a memorization element.

IN THE ABSTRACT

Please rewrite the abstract as shown below.

~~**MONOTONOUS COUNTER USING MEMORY CELLS**~~**ABSTRACT**

ABSTRACT

A ~~**monotonous**~~ **monotonic** counter formed as an integrated circuit, each counting bit being provided by a memory cell containing at least one ~~**memorization**~~ **storage** element formed of a polysilicon resistor, programmable by irreversible decrease in its value.

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A ~~monotonous~~ monotonic counter formed as an integrated circuit, each counting bit being provided by a memory cell ~~(11, 11'; 11")~~ containing at least one ~~memorization~~ storage element ~~(Rp; Rp1, Rp2)~~ formed of a polysilicon resistor, programmable by irreversible decrease in its value.

2. (Currently Amended) The counter of claim 1, wherein the programming of said resistor ~~(Rp; Rp1, Rp2)~~ is performed by temporarily submitting it to a constraint current greater than a current for which its value exhibits a maximum.

3. (Currently Amended) The counter of claim 1, comprising a circuit ~~(30)~~ for decoding the states contained in said cells ~~(11, 11'; 11")~~ for providing the resulting count.

4. (Currently Amended) The counter of claim 1, wherein each counting cell ~~(11")~~ comprises, in parallel between two terminals ~~(12, 13)~~ of application of a supply voltage ~~(Vp, Vr)~~, two branches each comprising:

a first polysilicon programming resistor ~~(Rp1, Rp2)~~ connected between a first supply terminal ~~(12)~~ and a terminal of differential reading ~~(24, 26)~~ of the cell state; and

at least one programming switch ~~(MN1, MN2)~~ connecting one of said read terminals to the second supply terminal ~~(13)~~.

5. (Original) The counter of claim 4, wherein each branch comprises a programming switch.

6. (Currently Amended) The counter of claim 4, wherein said programming resistors ~~(Rp1, Rp2)~~ are two polysilicon resistors identical in size and in possible doping.

7. (Currently Amended) The counter of claim 1, wherein each counting cell ~~(11, 11')~~ comprises a programming transistor ~~(MN, MP)~~ in series with a programming resistor

~~(Rp)~~.

8. (Currently Amended) The counter of claim 1, further comprising a circuit for controlling the programming of each of the counting cells ~~(11, 11'; 11")~~, capable of providing individual control signals to the programming switches.

REMARKS

This is a preliminary amendment in which the specification and claims have been amended to place them in better form before initial examination by the Examiner.

A favorable action is earnestly solicited.

Respectfully submitted,

Luc WUIDART

By: _____

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